

# Functional tests and selection of detectors for JEDI

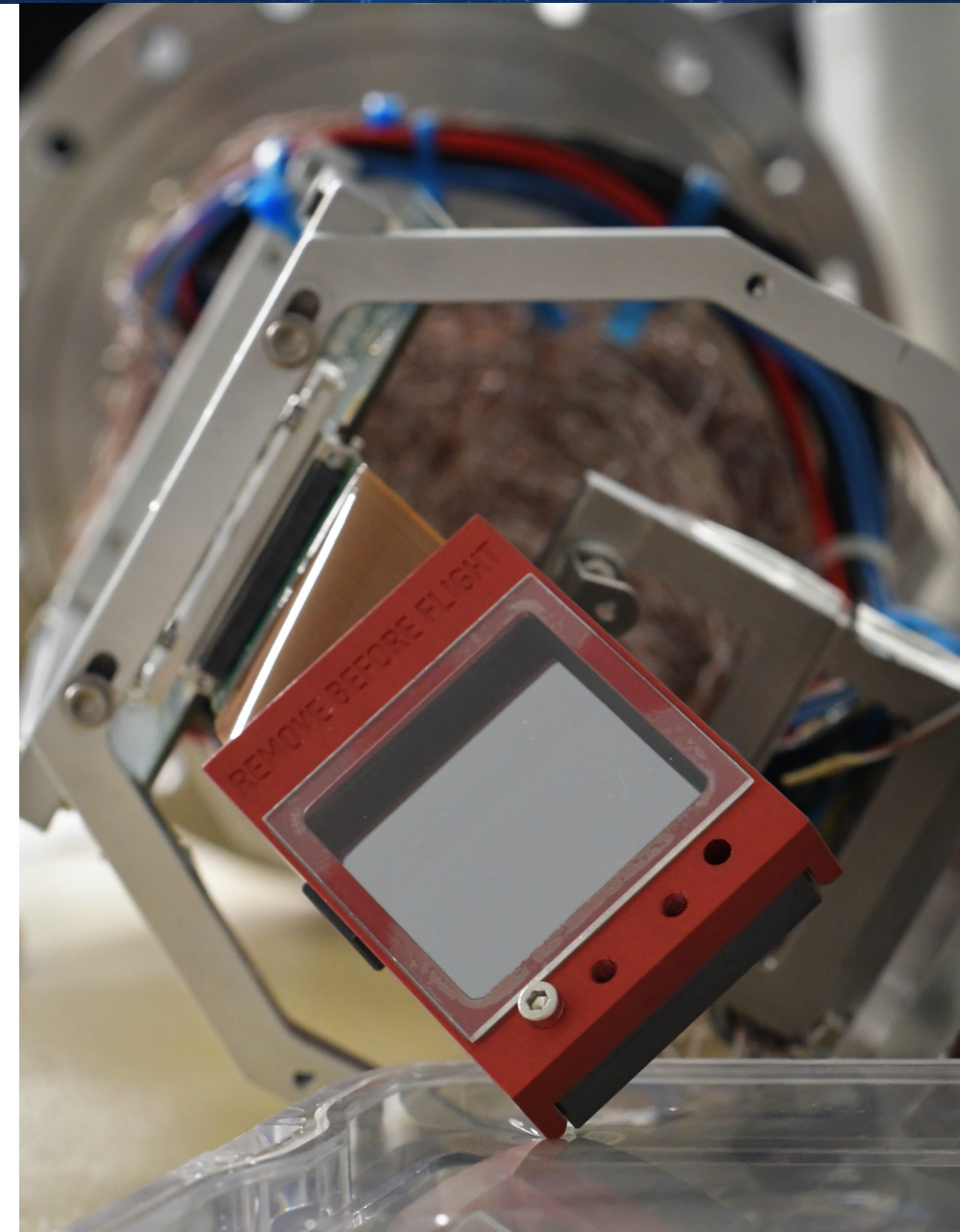
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together with ROB & CSL teams

Orsay, 5-6 May 2025

# Main motivation

- To select the best “EUI” detector among ~10 available CMOS-BSI detectors\* and provide basic characterization of its functionality.

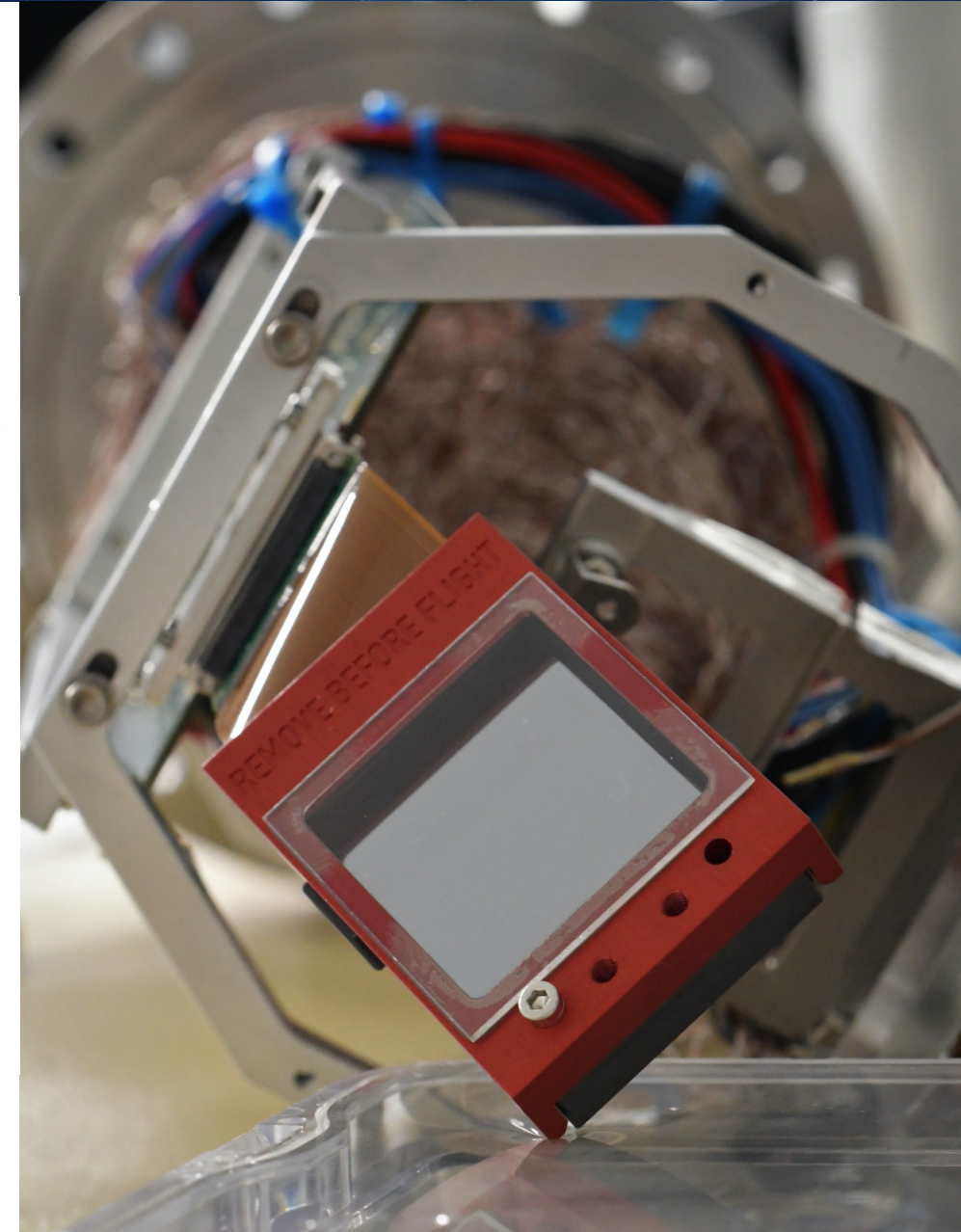
\* they are already stored in the CSL in a clean room (ISO 5) and ready for testing





# Requirements comparison to heritage

<u>Characteristic</u>	EUI detector	PROJECT Requirement	Heritage Margin to PROJECT Req
Detector Format	3072 x 3072	3k x 3k	Complies
Pixel Pitch:	10 $\mu\text{m}$	10 $\mu\text{m}$	Complies
Full <u>Well</u> Charge:	> 80 <u>ke</u> (LG), > 5 <u>ke</u> (HG)	>80 <u>ke</u> (LG)	Complies
Dynamic Range:	> 84 dB (dual gain) @ -40°C		
Dark Current:	< 5 e/s/pix at -20°C	0.05 e/sec/pix at -50 °C (?)	
Readout Noise	< 5 e (HG) , < 50 e (LG)	2.8 e (HG) ?	
Radiation Hardness	100 <u>krad</u>	>50 <u>krad</u>	Complies
Operational Temp.	-60 / -40 °C	-60 / -40 °C	Complies
Output Read Rate:	13.6 <u>Msp</u> s (1.5 <u>fps</u> 3kx3k)		



# EUI BSI detectors will be submitted to the following tests:

## 1. Functional Test

(this is the first test that will be applied to all available detectors in order select the best ones for the further, more detailed tests)

- Dark current measurements taken at **different integration time** and at **ambient** temperature
  - Expected results:
    - Dark noise as a function of integration time
    - Number and type of defects (bright/dark pixels, rows etc)
    - Power consumption (**should be less than 1 watt of power**)



# EUI BSI detectors will be submitted to the following tests:

## 2. Detector Performance Tests

(those are the tests that will be applied to the "short-listed" detectors in order select the best "flying" one)

- Noise evaluation (different integration time and different temperatures)
  - Bias
  - Dark current map
  - Stability assessment (dark and under illumination, very long integration time)
- Optical sensitivity evaluation (different integration time and different temperatures)
  - Non-Linearity (depends on the gain level) and Conversion Factor (possible with the optical source)
  - Flat-field measurements (only with the EUV source)

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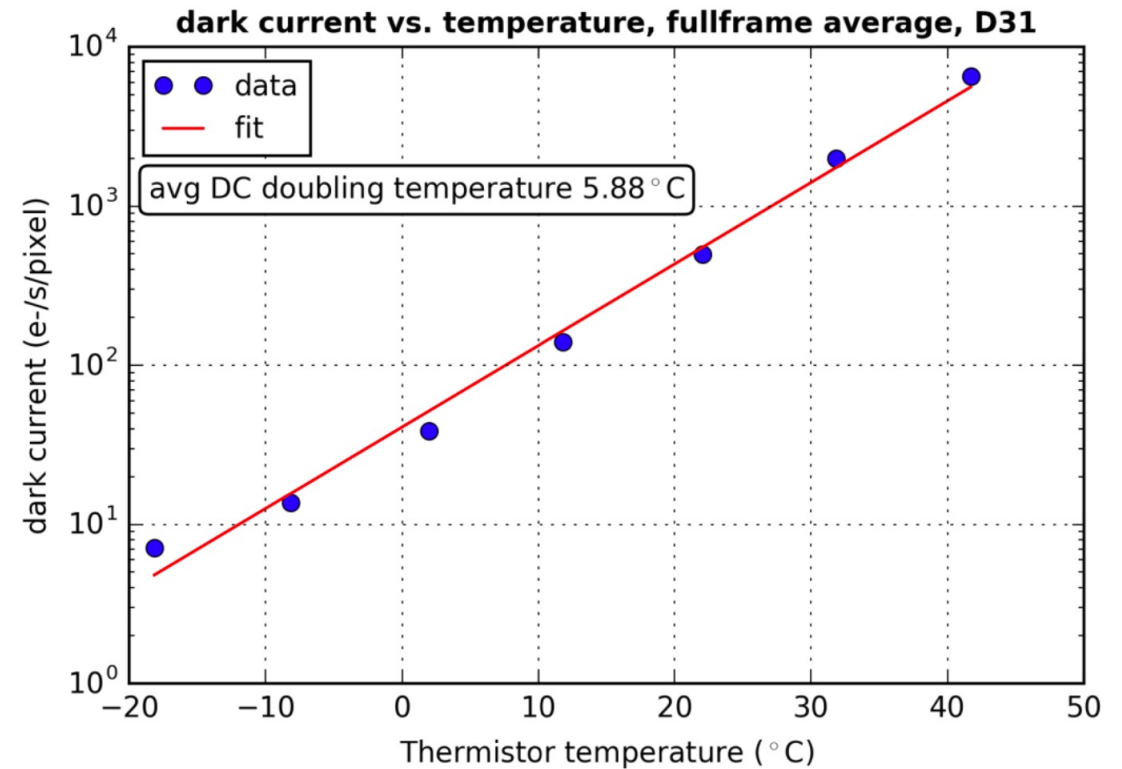


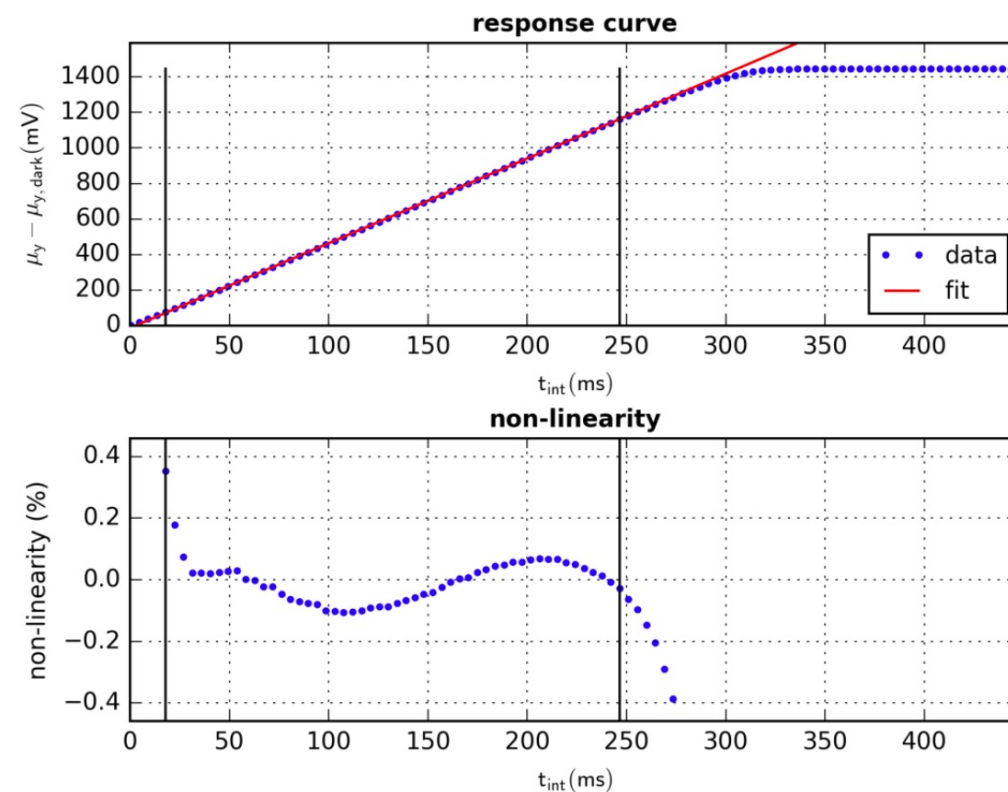
Figure 15: Dark current as function of temperature for BSI CoB D31.

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Signal = bias level (*temperature*) +

dark current level (*integration time, temperature, gain mode*) +

readout noise (*gain mode*) +





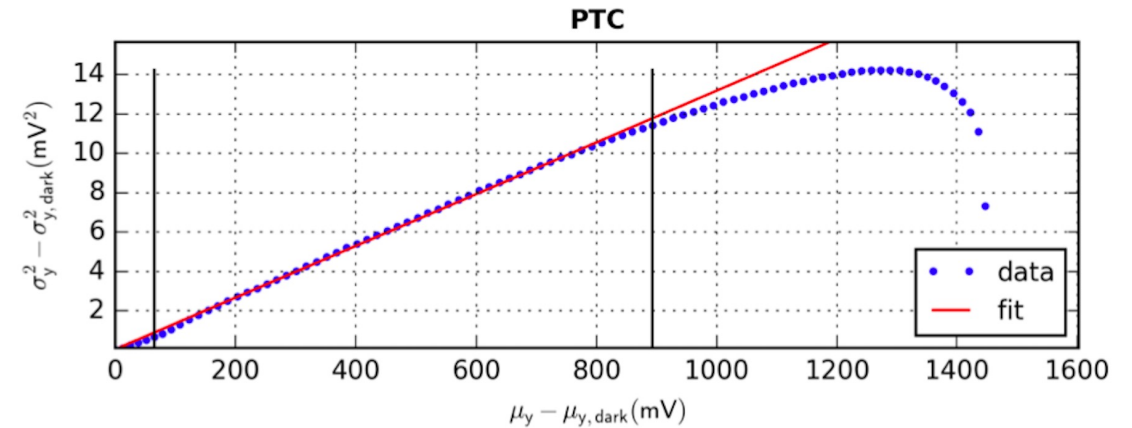
Let's define the signal from each pixel in the next way:

Signal = bias level (*temperature*) +

dark current level (*integration time, temperature, gain mode*) +

readout noise (*gain mode*) +

the number of photoelectrons read out at the output of the chip (*integration time*)



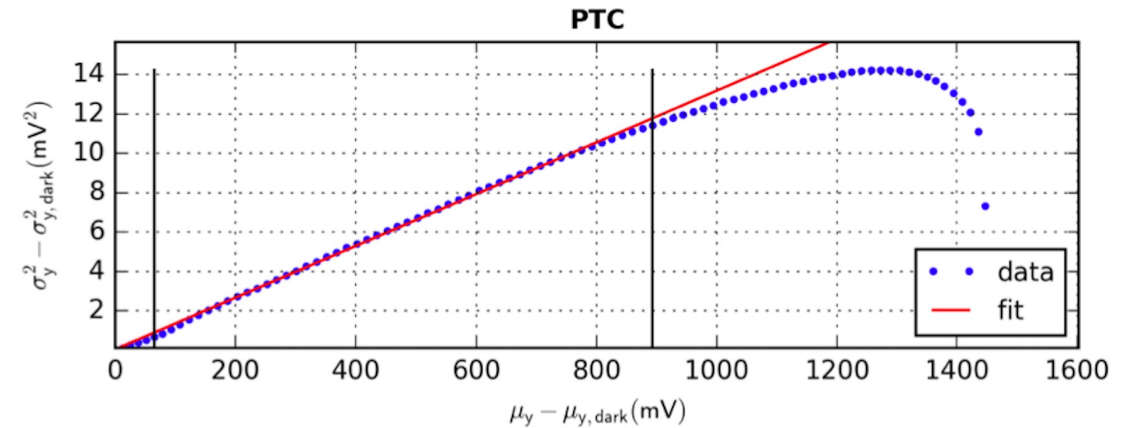
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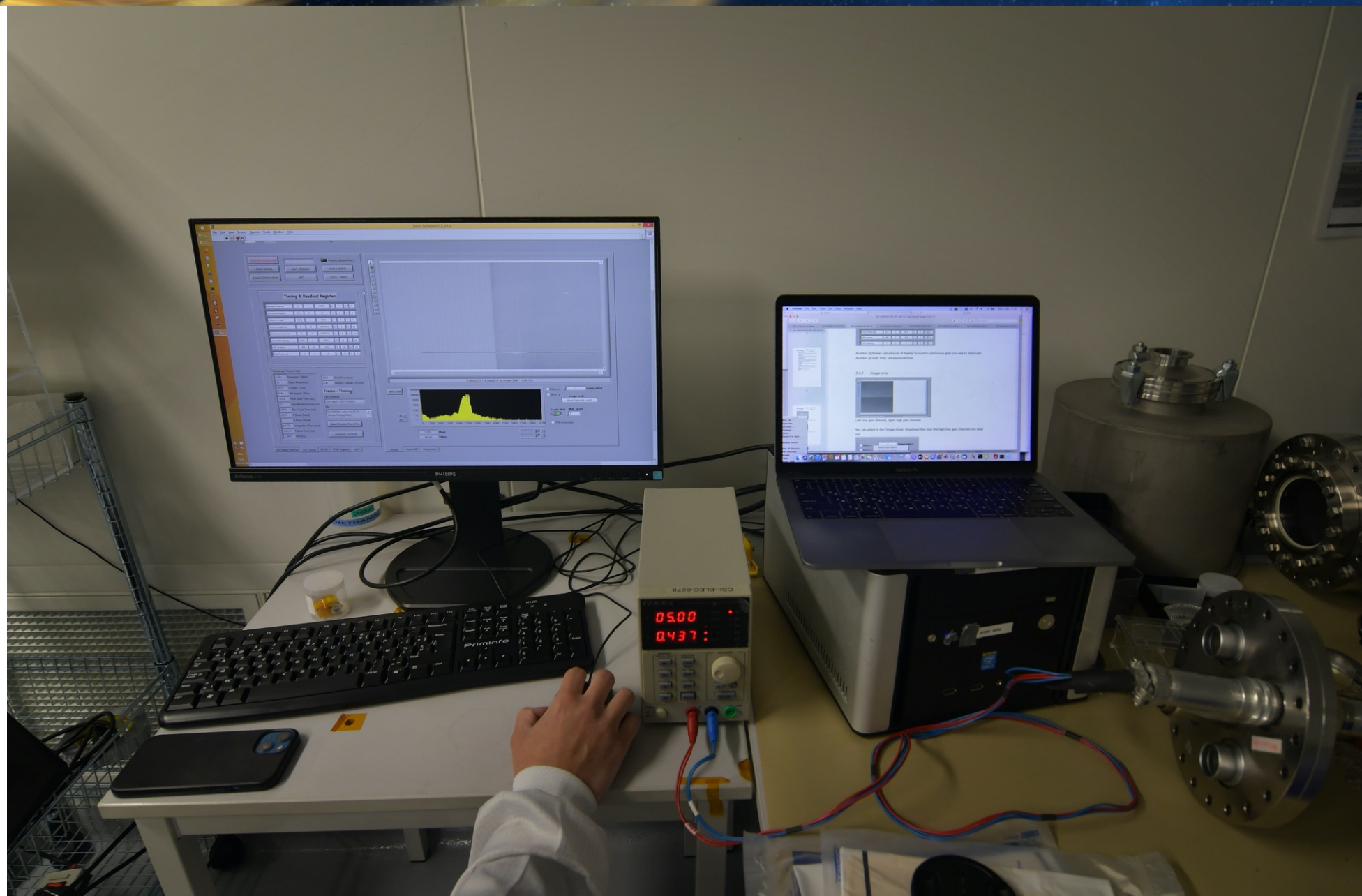
What we have learned from the previous missions (EUI, ASPIICS):

- bias is not constant
- significant non-linearity depending on the gain mode (*we should not exceed the 2% threshold*)











Project Operate Tools Window Help

Demo Software EUJ\_V1.vi

STOP APPLICATION

GRAB SINGLE

GRAB CONTINUOUS

SAVE REGMAP

INIT

Vectors Update Req'd

SAVE CONFIG

LOAD CONFIG

Timing & Readout Registers

Number of frames	2	1	65535	0	1	0	16
Last Vector Address	221	0	511	0	2	0	9
Columns to read	3072	2	3072	0	3	0	12
Line nr of read start	0	0	16777215	0	4	0	24
Number of reset lines	2	1	16777215	0	5	0	24
Line nr of read stop	3071	0	3073	0	6	0	24
ADC clk phase	800	0	1023	0	8	0	10
Clock Frequency	0	0	3	0	10	0	2

Frame and Timing Info

<20>	Frequency [MHz]	2350	Grab Time [ms]
50	Clock Period [ns]	0.43	Approx. Display FPS [Hz]
3072	# Pixels / Row		
6144	# Samples / Row		
153.6	Row Read Time [us]		
55	Row Blanking Time [us]		
208.6	Row Total Time [us]		
3072	# Rows [Read]		
2	# Rows [Reset]		
0.4172	Integration Time [ms]		
640.819	Frame Time [ms]		
1.5605	FPS [Hz]		

Frame - Timing

Last updated

Sun, Apr 6, 2025 14:57:01

File

C:\SVN\EUI-software\V1.0\

Sensor Timing Files\

Select Vectors From File

Program To FPGA

6144x3072 0.15X Signed 16-bit image 2466 (26,376)

SAVE RAW

Mean

2466.7

Stddev

125.496

Mirror x

1

Image select

Mirror y

Image mode

Muxed Output Gain A and B

Enable Mult

Mult factor

1

FPN Correction

EUI Supply Settings

EUI Timing

EUI SPI

FPGA Registers

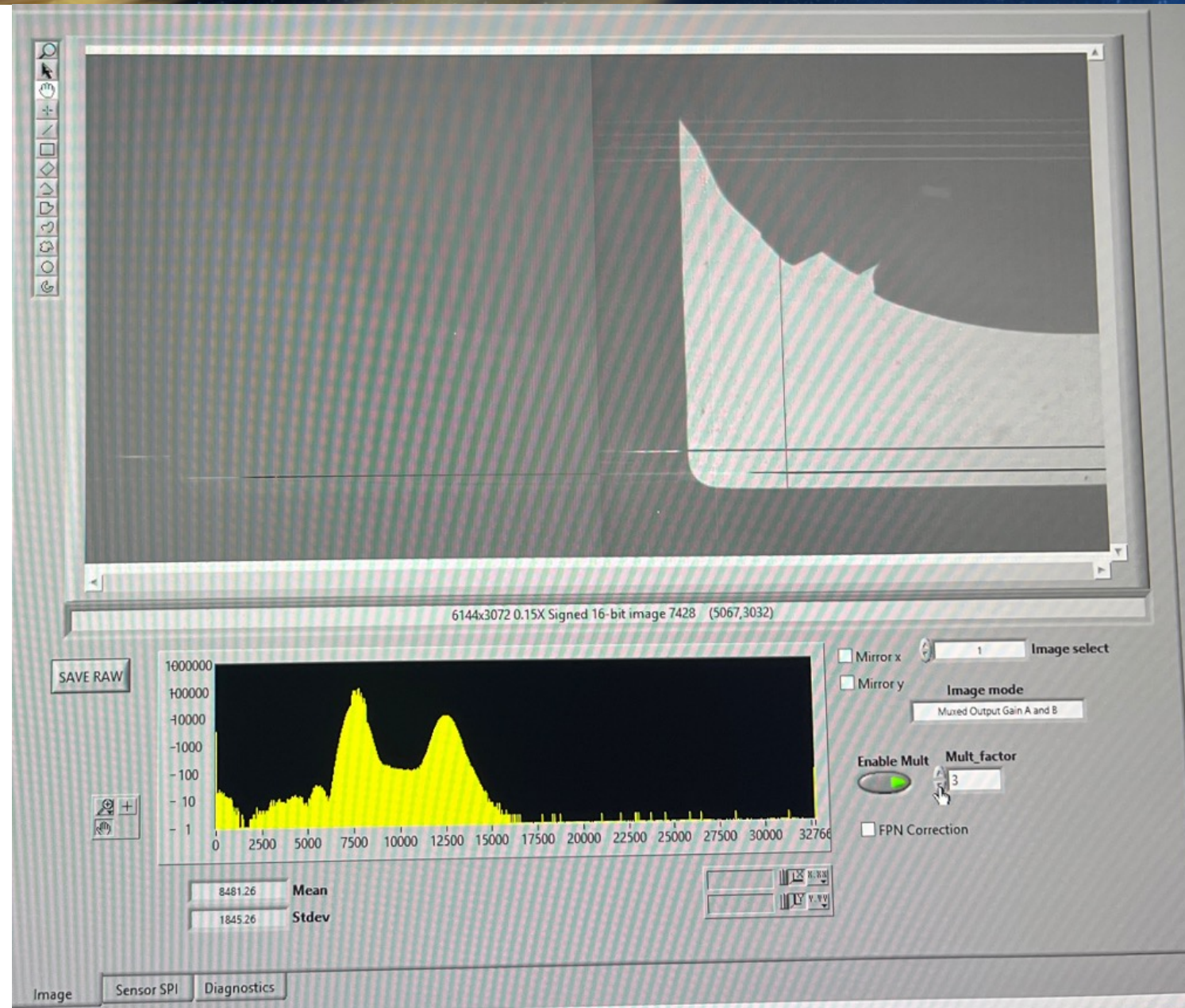
ADC

Image

Sensor SPI

Diagnostics





## We propose the next steps:

- To perform the functional tests for all available detectors at ambient temperature (ASAP);
- Depending on the number of short-listed detectors, put them in a vacuum chamber and perform different functional tests at various temperatures (check if the dark current measurements are in agreement with the previous “EUI” experiments);
- Perform the final flat-field measurements with the EUV source (Sergei’s calibration plan) for the best short-listed detectors.